Dual N-Channel 20V(S-S) MOSFET

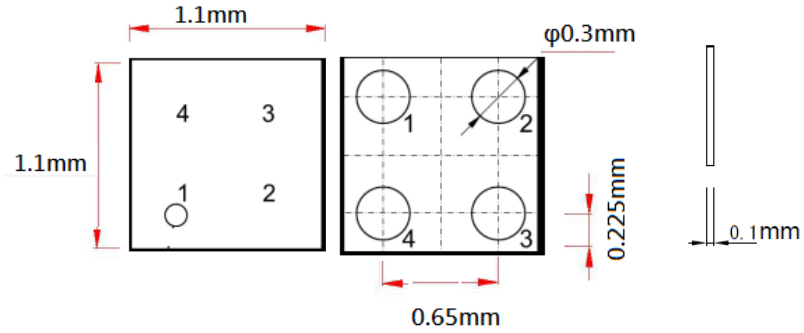
GENERAL DESCRIPTION

The FMW6622DW-G is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as notebook computer power management and other battery powered circuits where Low-side switching , and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- RSS(ON) ≦30 mΩ@VGS=4.5V
- RSS(ON) ≦32 mΩ@VGS=4.1V
- RSS(ON) ≦33 mΩ@VGS=4.0V
- RSS(ON) ≦34 mΩ@VGS=3.8V
- RSS(ON) ≦35 mΩ@VGS=3.7V
- RSS(ON) ≦38 mΩ@VGS=3.1V
- RSS(ON) ≦48 mΩ@VGS=2.5V
- Low Gate Charge
- Exceptional on-resistance and maximum DC current capability
- MSL=1

PIN CONFIGURATION



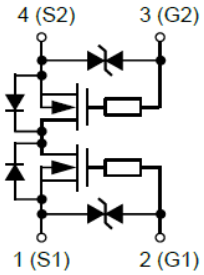
Unless otherwise specified,tolerances:x.xx±0.05(mm)

0.xx±0.03(mm)

Ordering Information: FMW6622DW-G(Green product-Halogen free)

APPLICATIONS

- Power Management
- DC/DC Converter
- Load Switch
- Battery Powered System



Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{SS}	20	V
Gate-Source Voltage		V_{GS}	±8	V
Continuous Drain Current*	T_A=25℃	I_D	6.5	A
	T_A=70℃		5.2	
Pulsed Drain Current*		I_{DM}	26	A
Maximum Power Dissipation*	T_A=25℃	P_D	2	W
	T_A=70℃		1.3	
Junction and Storage Temperature Range		T_J, Tstg	-55 to 150	℃
Thermal Resistance-Junction to Ambient *		$R_{\theta JA}$	62.5	℃/W

* Surface mounted on ceramic substrate (5000 mm2 x 0.8 mm).

Electrical Characteristics (T_J=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{(BR)SSS}$	Source-Source Breakdown Voltage	V_{GS}=0V, Is=1mA	20			V
$V_{GS(th)}$	Gate Threshold Voltage	Vss=10V, Is=0.16mA	0.35		1.4	V
I_{GSS}	Gate Leakage Current	Vss=0V, V_{GS}=±8V			±1	μA
		Vss=0V, V_{GS}=±3.8V			±0.1	
I_{SSS}	Zero Gate Voltage Source Current	Vss=20V, V_{GS}=0V			1	μA
$R_{SS(ON)}$	Source-Source On-State Resistance[a]	V_{GS}=4.5V, Is= 1.7A	20	23	30	mΩ
		V_{GS}=4.1V, Is= 1.7A	20.5	24	32	
		V_{GS}=4.0V, Is= 1.7A	20.5	24	33	
		V_{GS}=3.8V, Is= 1.7A	21	24.5	34	
		V_{GS}=3.7V, Is= 1.7A	21.5	25	35	
		V_{GS}=3.1V, Is= 1.7A	24	27.5	38	
		V_{GS}=2.5V, Is= 1.7A	25	33	48	
$V_{F(S-S)}$	Forward Source-Source Voltage	Is=1.7A, V_{GS}=0V			1.2	V

Notes: a. pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

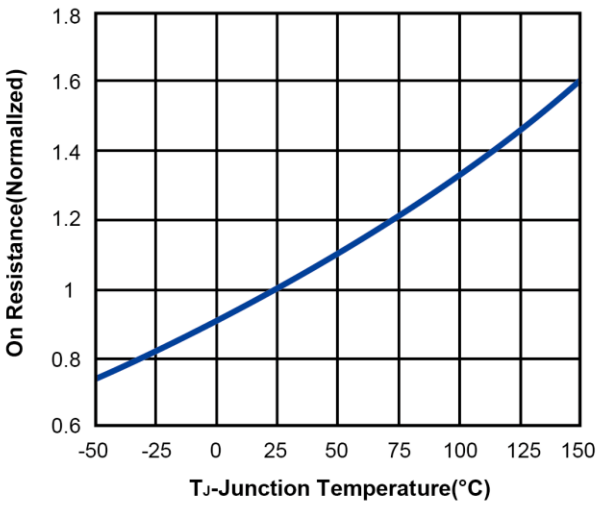
b. Force mos reserves the right to improve or change product design, functions, reliability, qualified manufacturer without notice.

DYNAMIC						
Qg	Total Gate Charge	Vss=10V, V_{GS}=4V, I_D=4A		9.9		nC
Qgs	Gate-Source Charge			3		
Qgd	Gate-Drain Charge			2.6		
Ciss	Input Capacitance	Vss=10V, V_{GS}=0V F=1MHz		697		pF
Coss	Output Capacitance			70		
Crss	Reverse Transfer Capacitance			41		
$t_{d(on)}$	Turn-On Delay Time	Vss=10V, R_L =10Ω V_{GS}=4V,R_G=3.3Ω Is=1A		200		ns
t_r	Turn-On Rise Time			367		
$t_{d(off)}$	Turn-Off Delay Time			1467		
t_f	Turn-Off Fall Time			831		

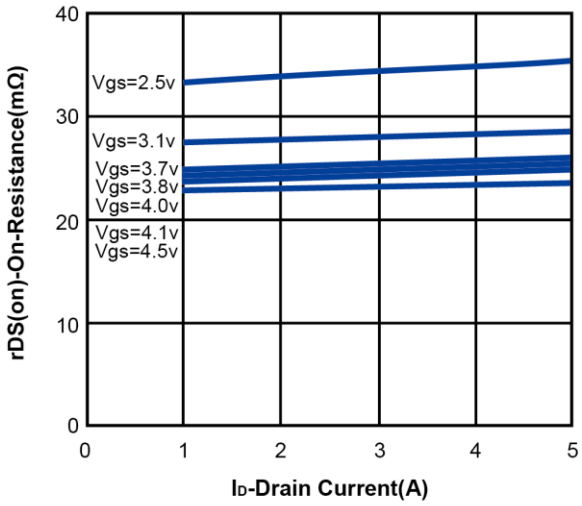
Notes: Switching time test circuit and waveform are based on MIL-STD-750E Measuring methods

Typical Characteristics (T_J =25℃ Noted)

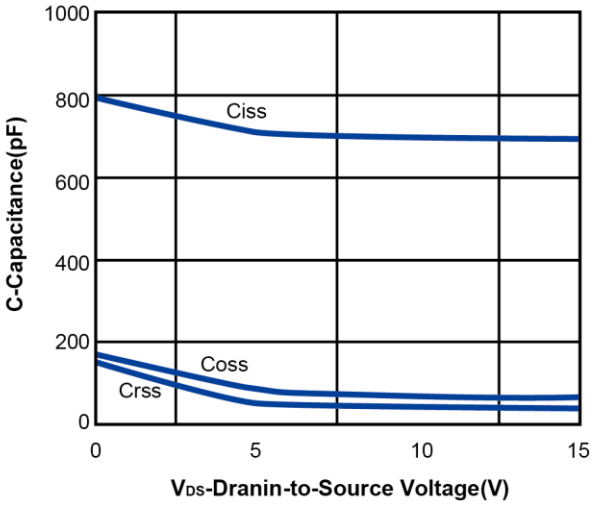
On Resistance vs. Junction Temperature



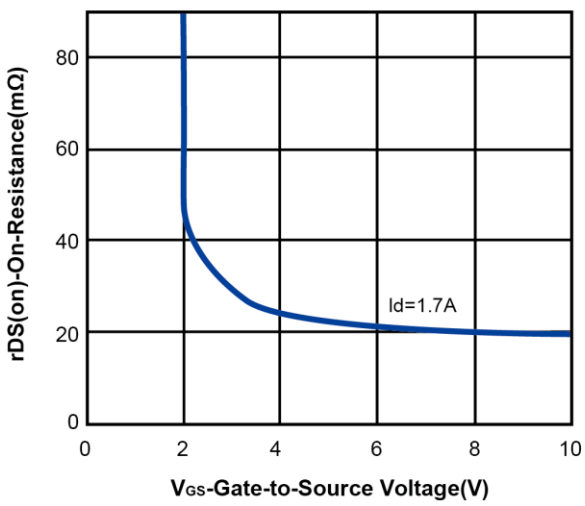
On Resistance vs. Drain Current



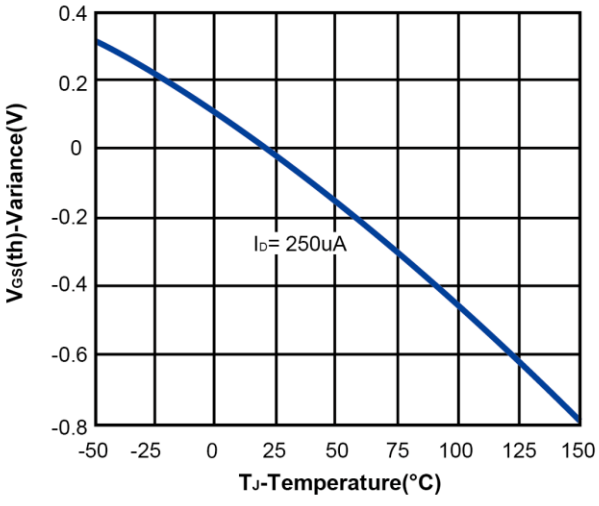
Capacitance



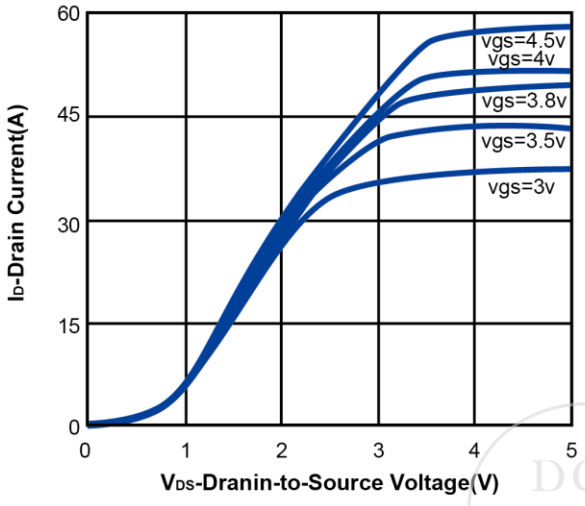
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage



On-Region Characteristics



Typical Characteristics (T_J =25℃ Noted)